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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,785	04/14/2006	Kensuke Takahashi	03680036AA	3566

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WHITHAM, CURTIS & CHRISTOFFERSON & COOK, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,785	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *21 and 27-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,22-26 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4-14-06; 12-6-07; 5-8-08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 14 April 2006.

Drawings

1. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see page 14, lines 20-23). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The substitute specification filed on 14 April 2006 has not been entered because it does not conform to 37 CFR 1.125(b) and (c) because:

- It lacks the statement indicating that it includes no new matter;
- It is supposed to exclude the claims;
- The amended claims included with the substitute specification are not compliant with 37 CFR 1.126 because newly added claims have been given existing claim numbers and existing claims have been renumbered; and
- Each claim included with the substitute specification has not been provided with the proper status identifier.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Semiconductor Device with Silicide-Containing Gate Electrode and Method for Fabricating the Same.

Claim Objections

5. Claims 21, 27-30 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple

dependent claim. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuo et al. (US 2003/0143825 A1 – from applicant's IDS).

Referring to Fig. 3I and paragraphs [0051] to [0071], Matsuo et al. disclose a CMOS semiconductor device that includes a gate insulating film (110) formed on a silicon substrate (100), a tungsten silicide gate electrode (111) corresponding to an n-type transistor, and a tungsten silicide gate electrode (113) corresponding to a p-type transistor. The gate insulating film (110) can be a high k film like hafnium oxide (also see paragraphs [0028] to [0029]). As indicated in paragraph [0065], the composition of

the tungsten silicide gate electrode (111) corresponding to the n-type transistor has more silicon than tungsten (i.e x is less than 0.5), while the composition of the tungsten silicide gate electrode (113) corresponding to the p-type transistor has less silicon than tungsten (i.e x is greater than 0.5). Other metals, including nickel, can be substituted for tungsten as indicated in paragraph [0070].

These are all of the limitations as set forth in claims 1-2, 8-9 of the applicant's invention.

8. Claims 1-20, 22-26, 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Kittl (US 2006/028156 A1).

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15. It is noted that the application papers filed on 14 April 2006 include a declaration indicating that the originally filed specification and claims are an exact translation of PCT/JP05/11331 filed on 21 June 2005. However, there is no such declaration for the Japanese priority document, Japanese application number 2004-184758 filed on 23 June 2004.

Referring to paragraphs [0054] to [0144], Kittl discloses fully silicided gate structures that include a high k gate dielectric material formed on a silicon wafer that can be hafnium silicon oxynitride or a hafnium silicon oxynitride/silicon dioxide stack and a nickel silicide gate electrode formed on the high k gate dielectric material (see paragraph [0098]). As indicated in Figs. 11-12 and paragraph [0067], the gate

structures can utilize various phases of nickel silicide including Ni_3Si (i.e. x = 0.75), which can be used in PMOS applications, or NiSi (i.e. x = 0.5), which can be used in NMOS applications.

These are all of the structural limitations as set forth in claims 1-20 of the applicant's invention.

Regarding the method claims, the nickel silicide gate electrodes are formed by blanket depositing nickel over a polysilicon/gate dielectric stack, as indicated in paragraph [0084], which implies that the polysilicon is deposited and patterned, followed by thermal treatments and removal of unreacted metal by selective etching to form the fully silicided gate electrodes (see paragraphs [0054] to [0070]). Also, as indicated in paragraph [0084], the Ni_3Si phase is stable for nickel to polysilicon layer thickness ratios that are greater than 1.7 and the NiSi phase is stable for nickel to polysilicon layer thickness ratios that are between 0.6 and 1.0. Further, as indicated in paragraph [0103], the $NiSi_2$ phase is stable for nickel to polysilicon layer thickness ratios of about 0.3 to 0.35 when annealed at 800 degrees C.

These are all of the process limitations as set forth in claims 22-26, 31 of the applicant's invention.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al. (US 2003/0143825 A1 – from applicant's IDS) as applied to claim 1 above, and further in view of Li (US 2005/0280104 A1) and Colombo et al. (US 7,098,516 B2).

As shown above Matsuo et al. anticipate claim 1 of the applicant's invention. However, Matsuo et al. do not expressly teach or suggest a plural layered gate insulator (limitations of claims 3-4, 6-7), nor a gate insulator that includes hafnium silicon oxynitride (limitations of claims 5-7). Li teaches alternative high k gate dielectric layers to hafnium oxide as well as multi-layered high k gate dielectric layers that can include silicon dioxide or silicon nitride (see paragraph [0037]). Colombo et al. teach a hafnium silicon oxynitride high k gate dielectric layer (see column 5, lines 19-21).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Matsuo et al. by substituting other high k dielectric layers including multi-layered high k gate dielectrics, as taught by Li, and/or by specifically substituting hafnium silicon oxynitride, as taught by Colombo et al., for the hafnium oxide gate insulating film of Matsuo et al. because Li and Colombo et al. show that they have an art recognized equivalence as high k gate dielectric materials.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on Monday to Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen W Smoot/
Primary Examiner
Art Unit 2813

sws